REMARKS/ARGUMENTS

The Applicants originally submitted Claims 1-20 in the application. In a previous response and preliminary amendment, the Applicants amended Claims 1, 6, 8, 13-14 and 19. In the present response, the Applicants have amended independent Claims 1, 8 and 14 to more clearly indicate the invention and place the claims in condition for allowance. No claims have been canceled or added in the present response. Accordingly, Claims 1-20 are currently pending in the application.

I. Formal Remarks and Comments

As discussed with the Examiner during the interview, the present invention advantageously employs a single signal to add a delay that includes fixed delays associated with multiple of a plurality of taps. Figure 3 of the present application provides an embodiment of the present invention that clearly illustrates the pending language of independent Claims 1, 8 and 14. As noted, Figure 3 and the following discussion represent an embodiment of the invention and do not limit the scope of the pending Claims. Instead, the following discussion is presented to more clearly provide the Examiner with an understanding of pending Claims 1, 8 and 14.

FIGURE 3 illustrates an embodiment of a digital feedback delay line 250 including a plurality of taps 310, 320, 330, 340, 350, 360, 370, 380. In the illustrated embodiment, the digital feedback delay line 250 has 32 taps (only eight are actually shown, but ellipses between the 3rd tap 330 and the 15th tap 340, and the 16th tap 350 and the 30th tap 360 are intended to represent the remaining taps). Each of the plurality of taps 310, 320, 330, 340, 350, 360, 370, 380 is embodied in a 2:1 input multiplexer with input multiplexers cascaded, such that a signal appearing at an input of the 1st tap

310 is gated through to the input of the 2nd tap 320, and so on, until the signal is eventually gated out of the 32nd tap 380.

Tap selection logic in the illustrated embodiment includes a register 390 and a decoder 395. The decoder 395 receives the number programmed into the register 390, decodes it into a selection bit, and delivers the selection bit on one of 32 lines coupling the decoder 395 to respective ones of the plurality of taps 310, 320, 330, 340, 350, 360, 370, 380 (and those not shown). For example, if the register 390 contains a value of 16 (10000 binary), the decoder 395 decodes the number into a selection bit on the line that couples the decoder 395 to the 16th tap 350.

If the 32nd tap 380 is selected, the input signal VD_{in} is delayed by virtue of having to traverse only the 32nd tap 380 (yielding a minimum delay). If the 1st tap 310 is selected, the input signal VD_{in} is delayed by virtue of having to traverse all 32 taps (yielding a maximum delay). Accordingly, the tap selection logic, such as the register 390 and the decoder 395 in this embodiment, delivers a single signal (*i.e.*, that is the selection bit in this embodiment) to activate one of a plurality of taps (tap 310) and thereby insert a corresponding delay including fixed delays associated with multiple of the plurality of taps.

Language from the previous response is included below to demonstrate that Erickson does not teach delivering a single signal to activate one of a plurality of taps to insert a corresponding delay into a PLL wherein the corresponding delay includes fixed delays associated with multiple of the plurality of taps as recited in independent Claims 1, 8 and 14.

II. Rejection of Claims 1-20 under 35 U.S.C. §102

The Examiner has rejected Claims 1-20 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,815,016 to Erickson. The Applicants respectfully disagree.

Erickson does not teach delivering a single signal to activate one of a plurality of taps to insert a corresponding delay into a PLL wherein the corresponding delay includes fixed delays associated with multiple of the plurality of taps as recited in amended independent Claims 1, 8 and 14. Instead of a single signal able to insert a delay including fixed delays associated with multiple of a plurality of taps, Erickson teaches a single signal is used to add **a single delay element** to a delay path. In other words, each delay element is added to the delay path by a single corresponding signal.

Regarding Figure 1 and the corresponding discussion, Erickson discloses a phase-locked loop having a series of selectable voltage controlled delay elements (18, 19, 20) that can be inserted into a delay path at the choice of a user. (*See* column 4, lines 40-45 and Figure 1.) The voltage controlled delay elements are connected to a series of corresponding multiplexers (21, 22, 23) that are operated by control signals applied by a corresponding control element (24, 25, 26) to select or deselect a specific delay element or a combination of delay elements. As such, the delay elements may be introduced singly or may be cascaded. (*See* column 5, lines 4-12 and Figure 1.)

Thus, instead of delivering a single signal to activate one tap to insert a corresponding delay into a PLL wherein the corresponding delay includes fixed delays associated with multiple of the plurality of taps, Erickson discloses inserting each individual delay element into the delay path by a separate, corresponding control element. (*See* column 5, lines 4-12; column 7, lines 26-39; and Figure 1.) For example, delay element 20 is inserted into the delay path by control element 26 and

delay element 19 is inserted by control element 25. Thus, in Erickson, a single signal, such as from one of the control elements (24, 25, 26), does not insert a delay in the delay path wherein the delay includes multiple of the delay elements (18, 19, 20). (*See* Figure 1.) On the contrary, to add multiple delay elements to the delay path, Erickson requires a signal for each delay element. As such, Erickson fails to teach delivering a single signal to activate one of a plurality of taps to insert a corresponding delay including fixed delays associated with multiple of the plurality of taps as recited in amended independent Claims 1, 8 and 14.

Therefore, Erickson does not disclose each and every element of amended independent Claim 1, 8 and 14 and Claims dependent thereon. As such, Erickson does not anticipate independent Claims 1-20. The Applicants, therefore, respectfully request the Examiner to withdraw the §102 rejection with respect to Claims 1-20 and allow issuance thereof.

III. Conclusion

In view of the foregoing amendment and remarks, the Applicants now see all of the Claims currently pending in this application to be in condition for allowance and therefore earnestly solicit a Notice of Allowance for Claims 1-20.

The Applicants request the Examiner to telephone the undersigned attorney of record at (972) 480-8800 if such would further or expedite the prosecution of the present application. The Commissioner is hereby authorized to charge any fees, credits or overpayments to Deposit Account 08-2395.

Respectfully submitted,

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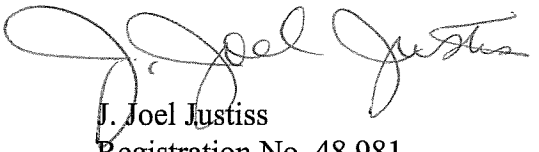

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